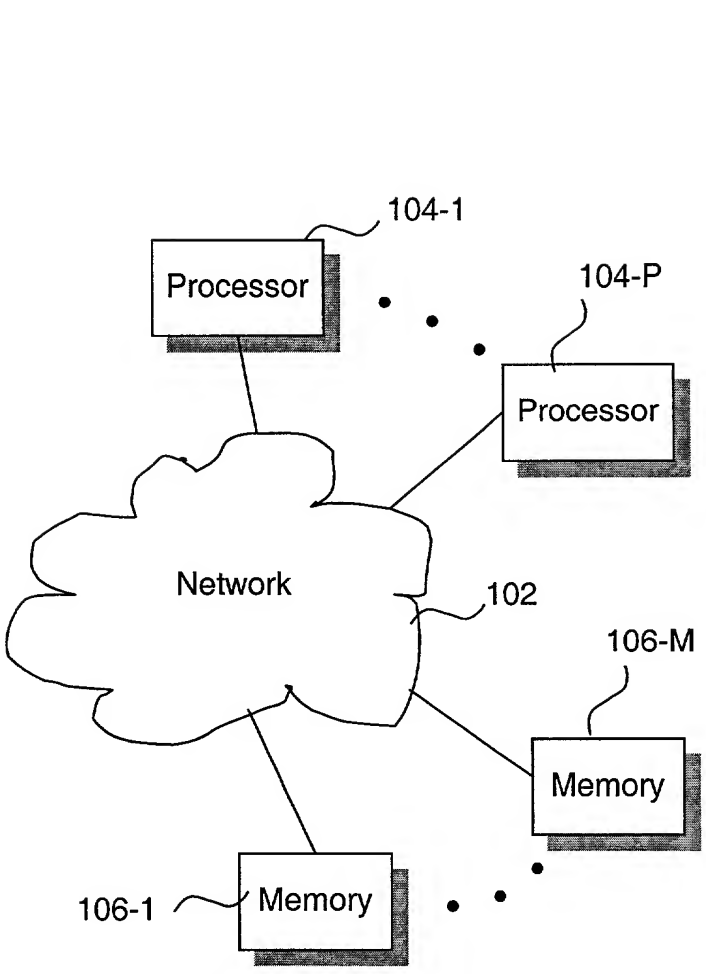
100
104-1
Processor
104-P
Processor
Network
102
106-M
Memory
106-1
Memory

FIG. 1

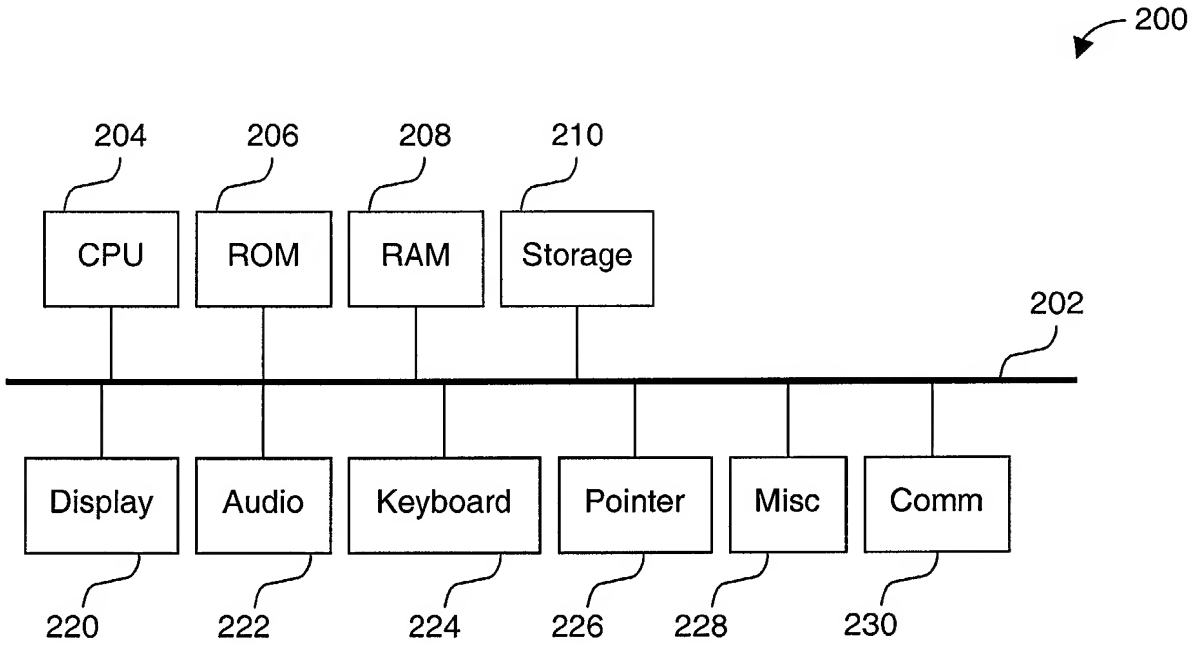
200
204
206
208
210
CPU
ROM
RAM
Storage
202
Display
Audio
Keyboard
Pointer
Misc
Comm
220
222
224
226
228
230

FIG. 2

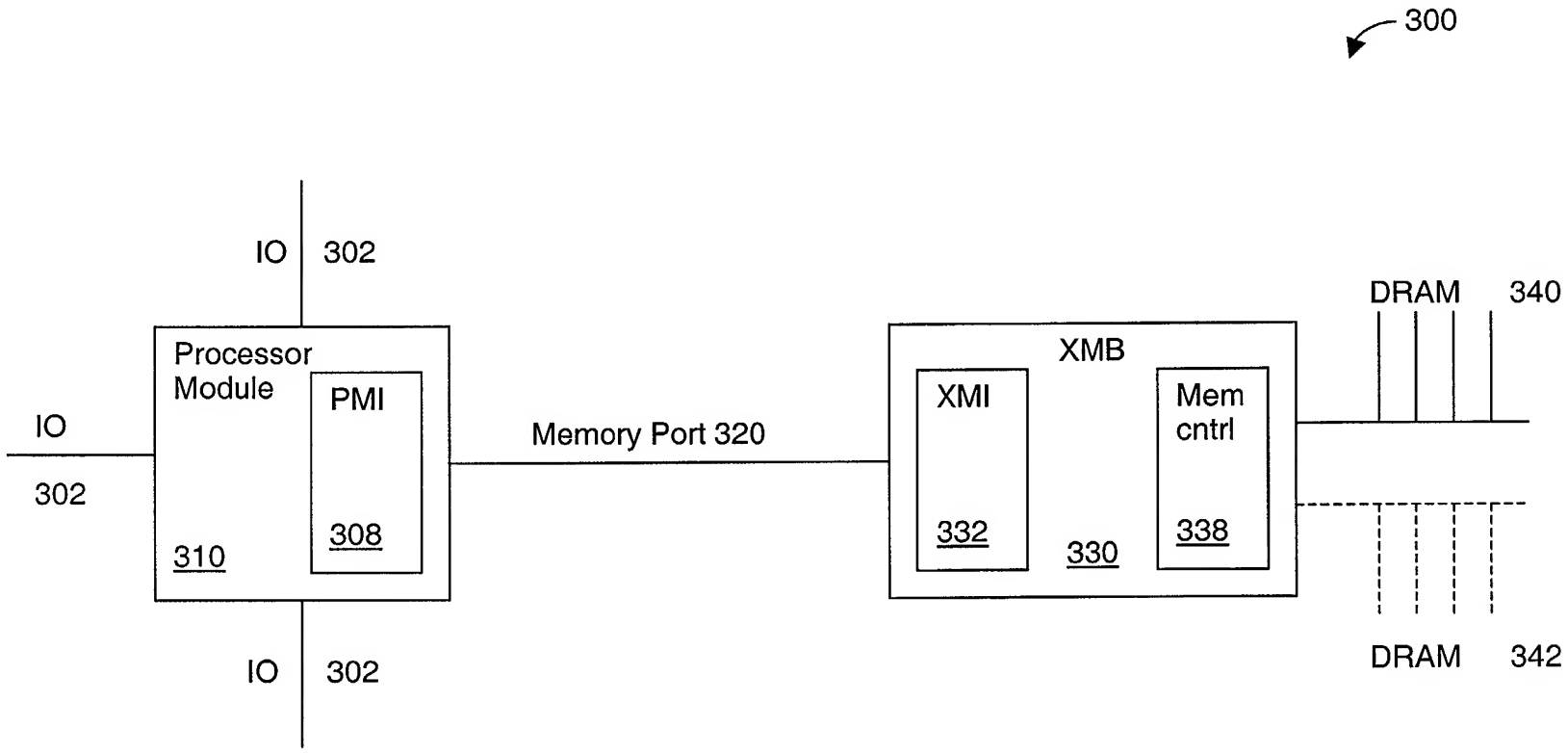
300
IO
302
Processor
Module
PMI
IO
302
310
308
Memory Port 320
XMB
XMI
332
330
Mem
cntrl
338
DRAM
340
DRAM
342
IO
302

FIG. 3

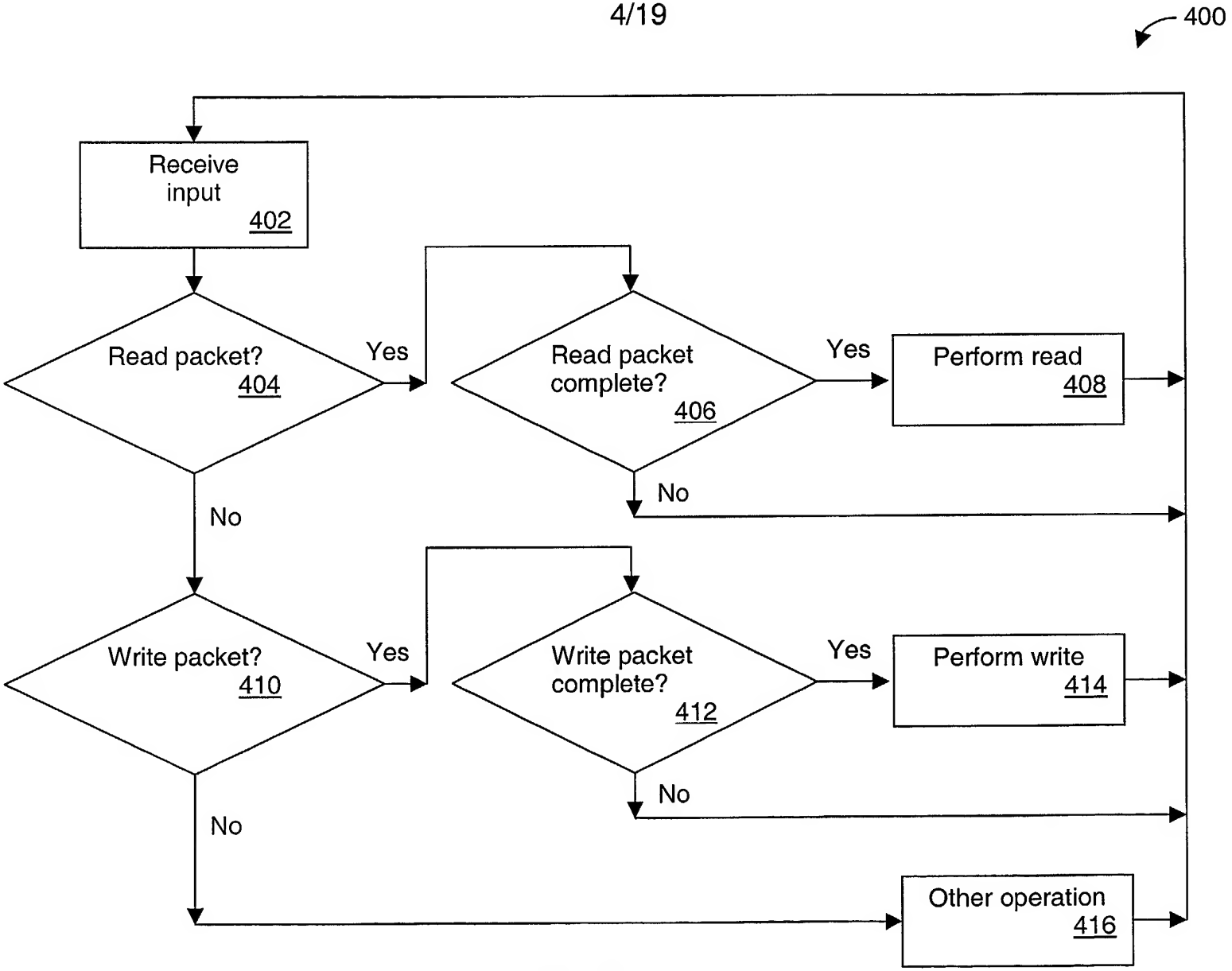
400
Receive input 402
Read packet? 404
Yes
Read packet complete? 406
Yes
Perform read 408
No
No
Write packet? 410
Yes
Write packet complete? 412
Yes
Perform write 414
No
No
Other operation 416

FIG. 4A

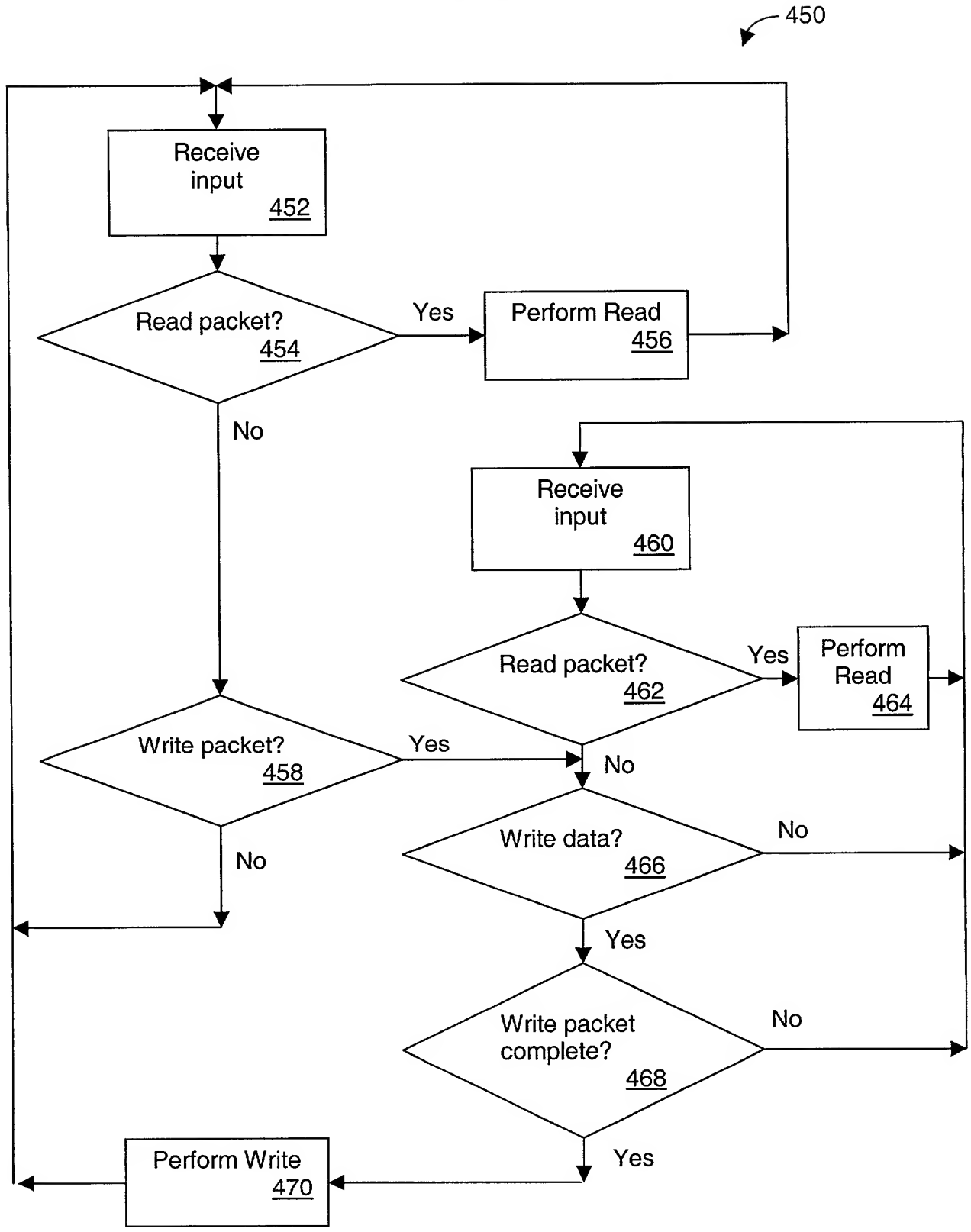
450
Receive input 452
Read packet? 454
Yes
Perform Read 456
No
Receive input 460
Read packet? 462
Yes
Perform Read 464
Write packet? 458
Yes
No
Write data? 466
No
No
Yes
Write packet complete? 468
No
Yes
Perform Write 470

FIG. 4B

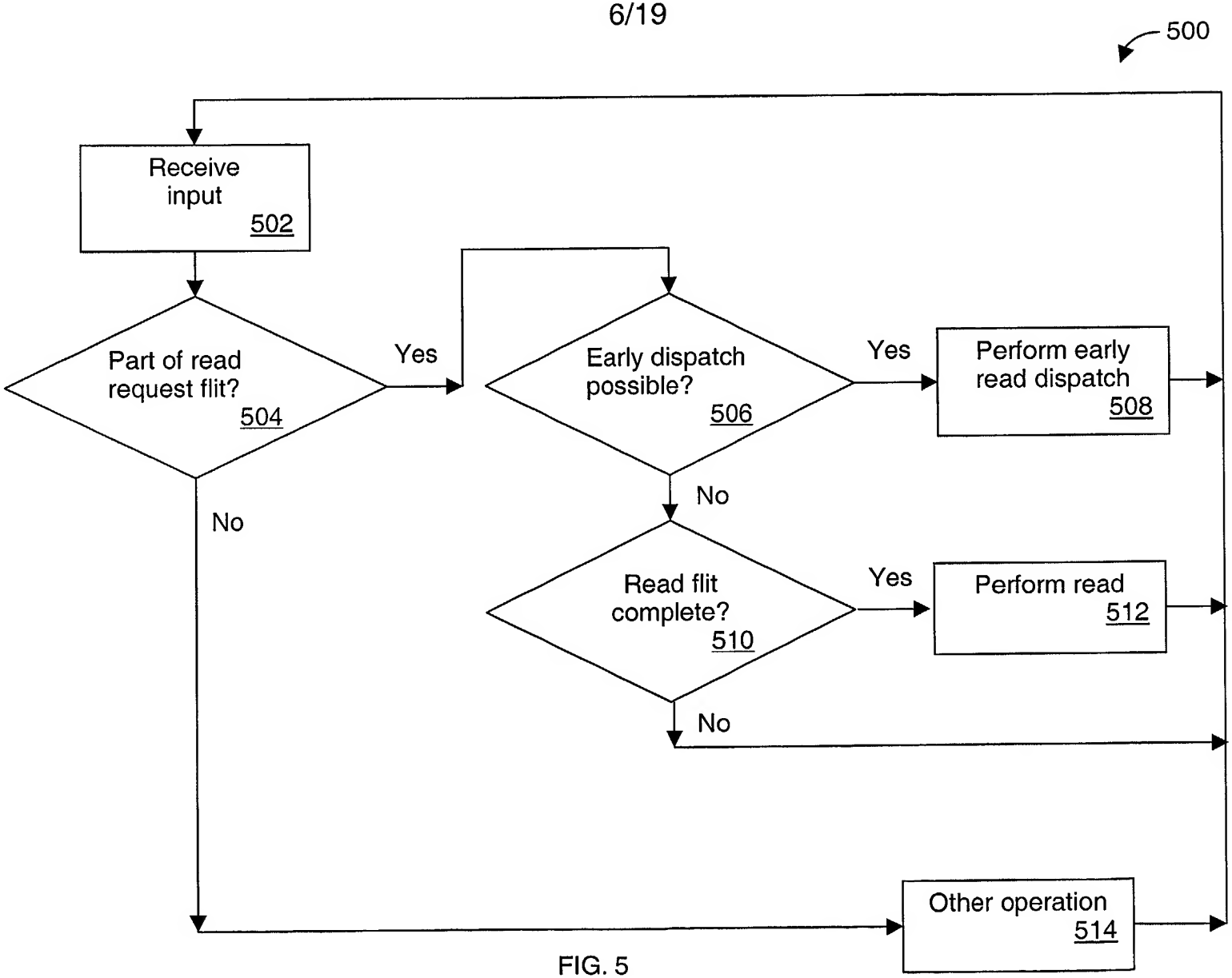
500
Receive input
502
Part of read request flit?
504
Yes
No
Early dispatch possible?
506
Yes
Perform early read dispatch
508
No
Read flit complete?
510
Yes
Perform read
512
No
Other operation
514

FIG. 5

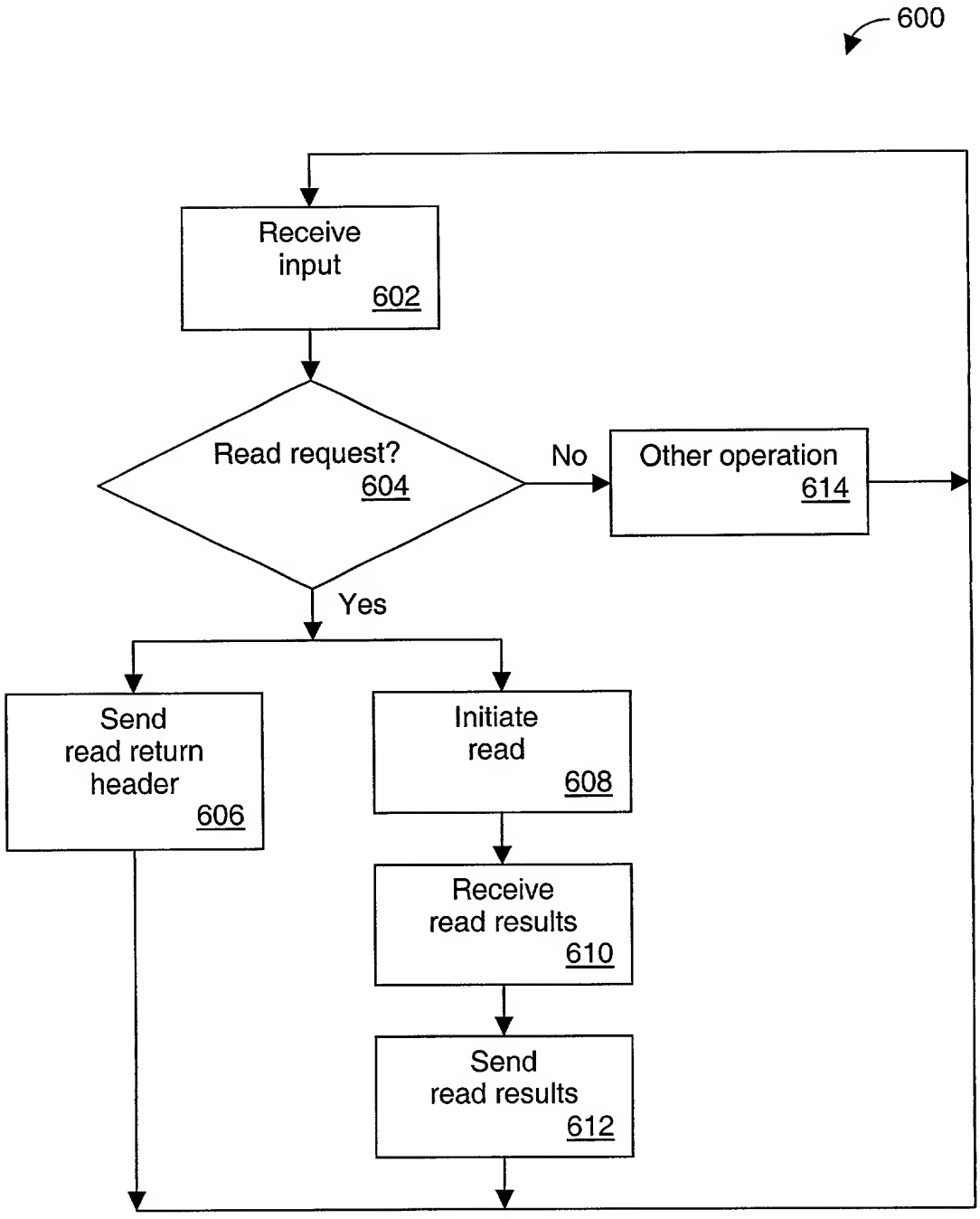
600
Receive input 602
Read request? 604
No
Other operation 614
Yes
Send read return header 606
Initiate read 608
Receive read results 610
Send read results 612

FIG. 6A

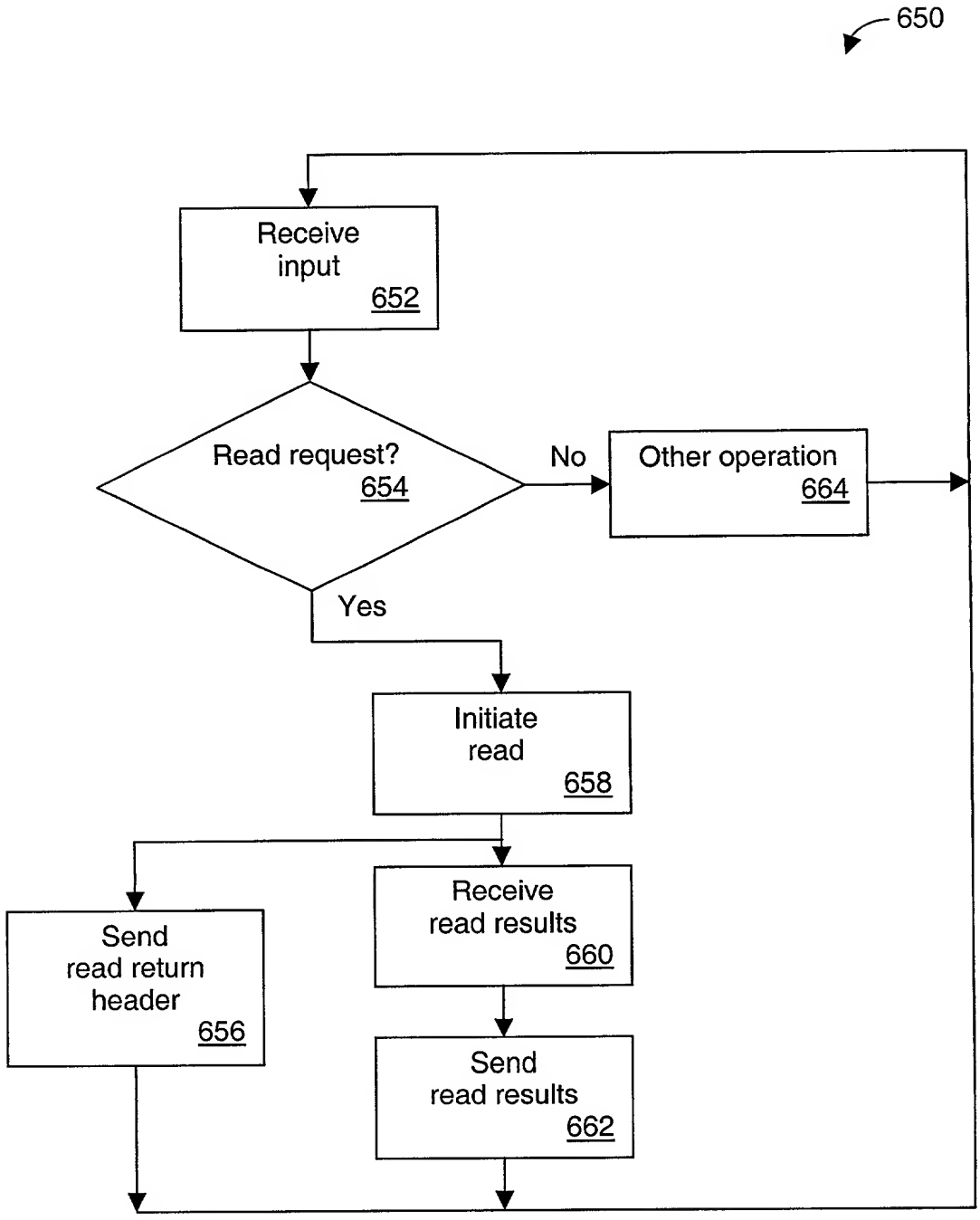
650
Receive input 652
Read request? 654
No
Other operation 664
Yes
Initiate read 658
Send read return header 656
Receive read results 660
Send read results 662

FIG. 6B

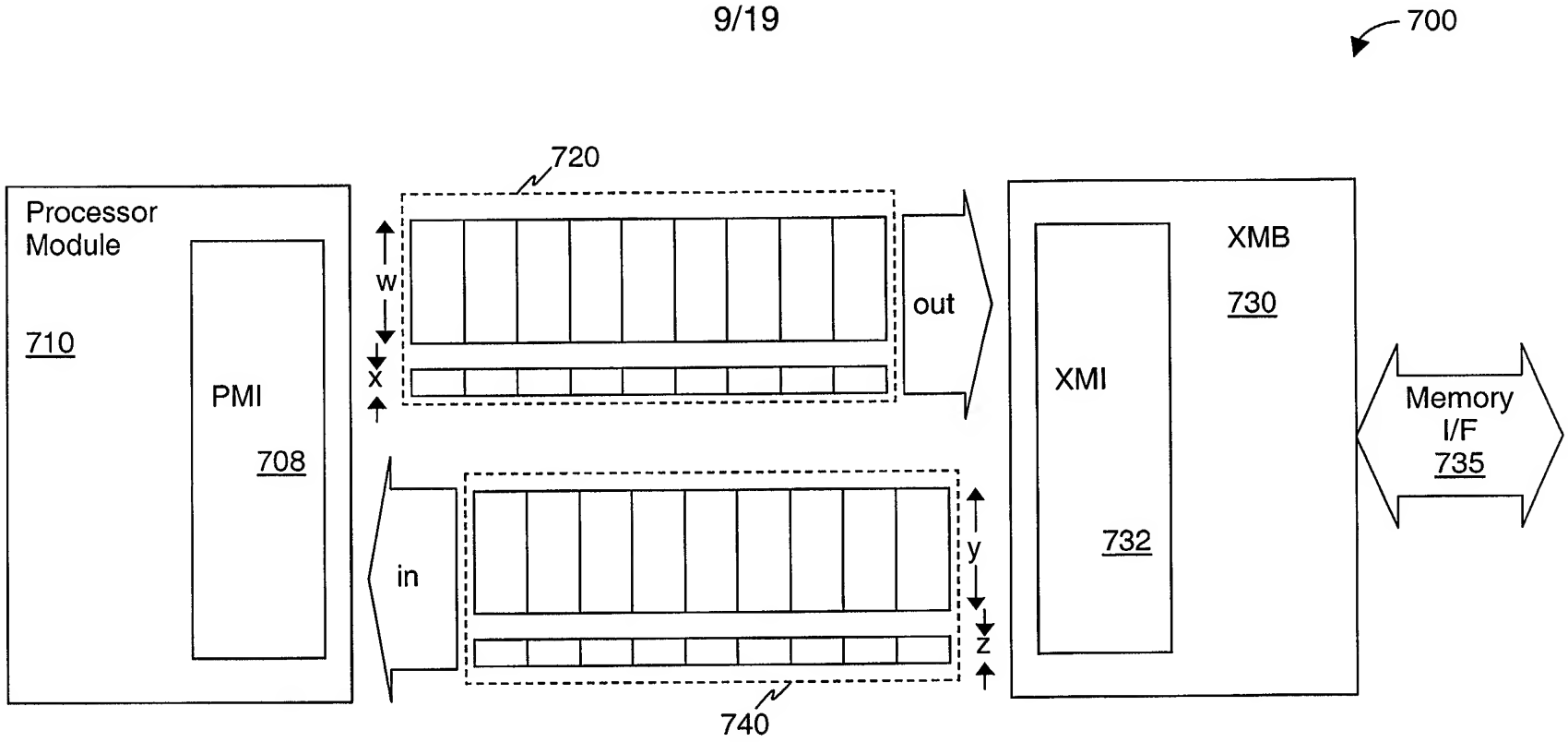
700
720
Processor Module
710
PMI
708
w
x
out
XMB
730
XMI
732
Memory I/F
735
in
y
z
740

FIG. 7

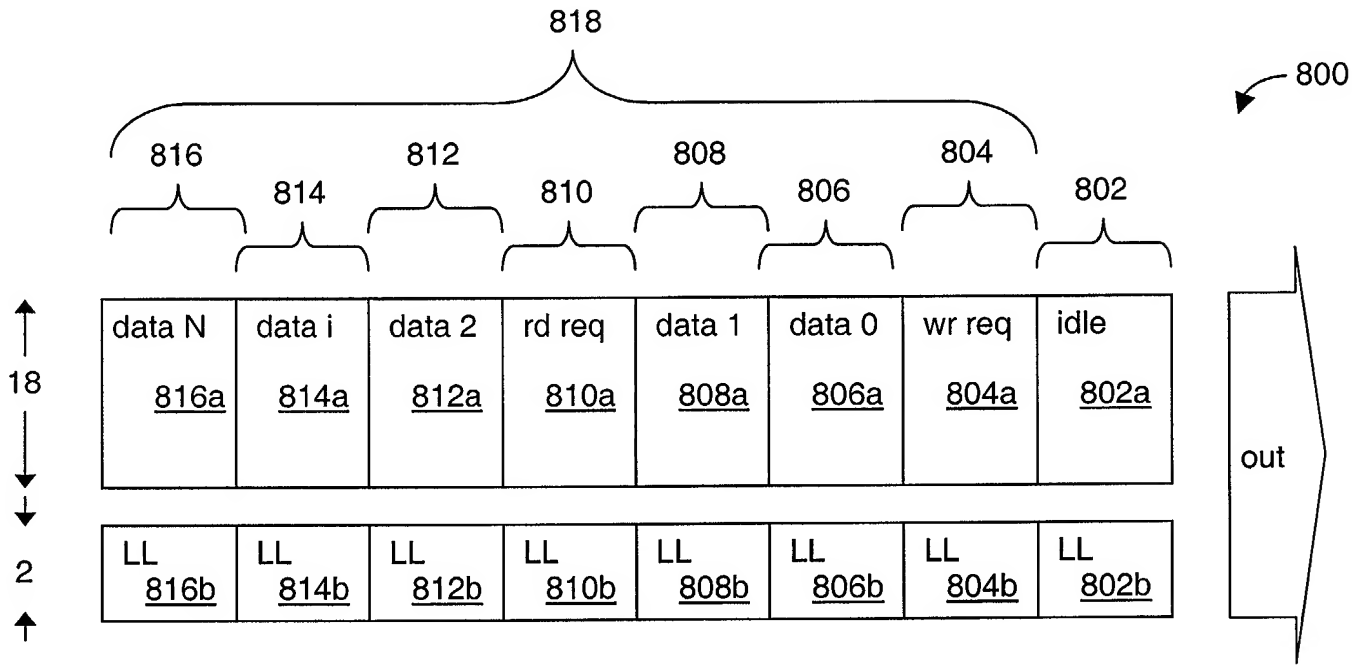
818
800
816
814
812
810
808
806
804
802
data N
816a
data i
814a
data 2
812a
rd req
810a
data 1
808a
data 0
806a
wr req
804a
idle
802a
18
2
LL
816b
LL
814b
LL
812b
LL
810b
LL
808b
LL
806b
LL
804b
LL
802b
out

FIG. 8

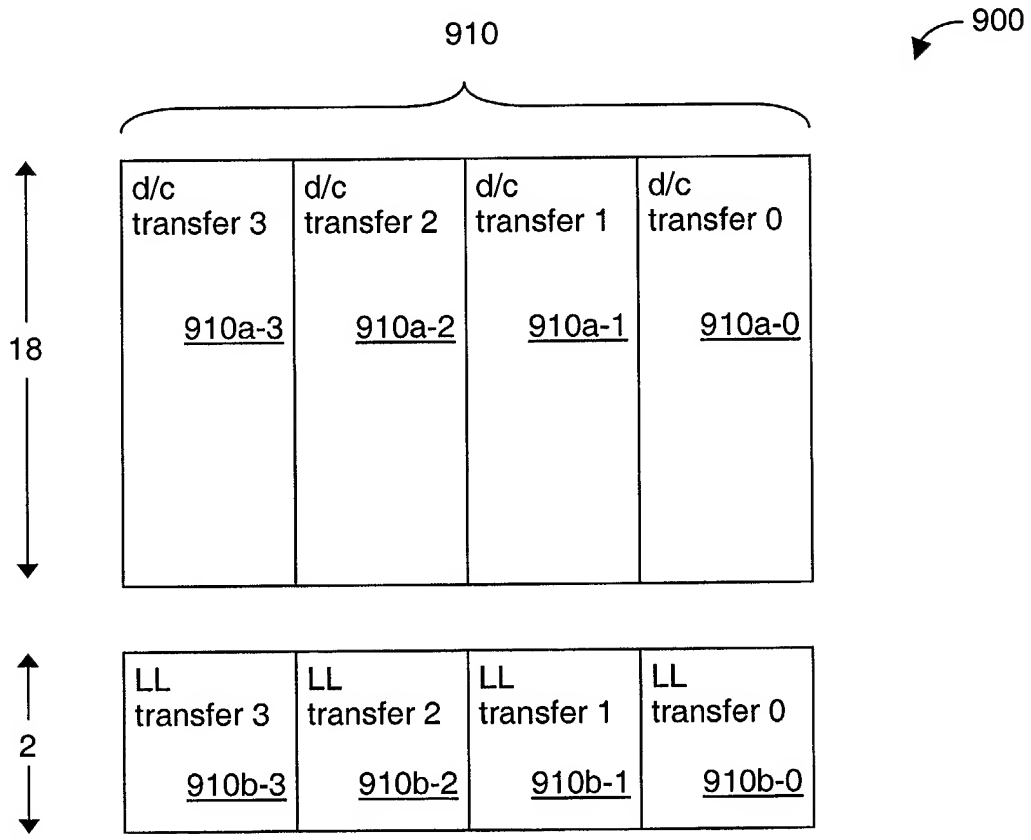
900
910
18
d/c transfer 3
910a-3
d/c transfer 2
910a-2
d/c transfer 1
910a-1
d/c transfer 0
910a-0
2
LL transfer 3
910b-3
LL transfer 2
910b-2
LL transfer 1
910b-1
LL transfer 0
910b-0

FIG. 9

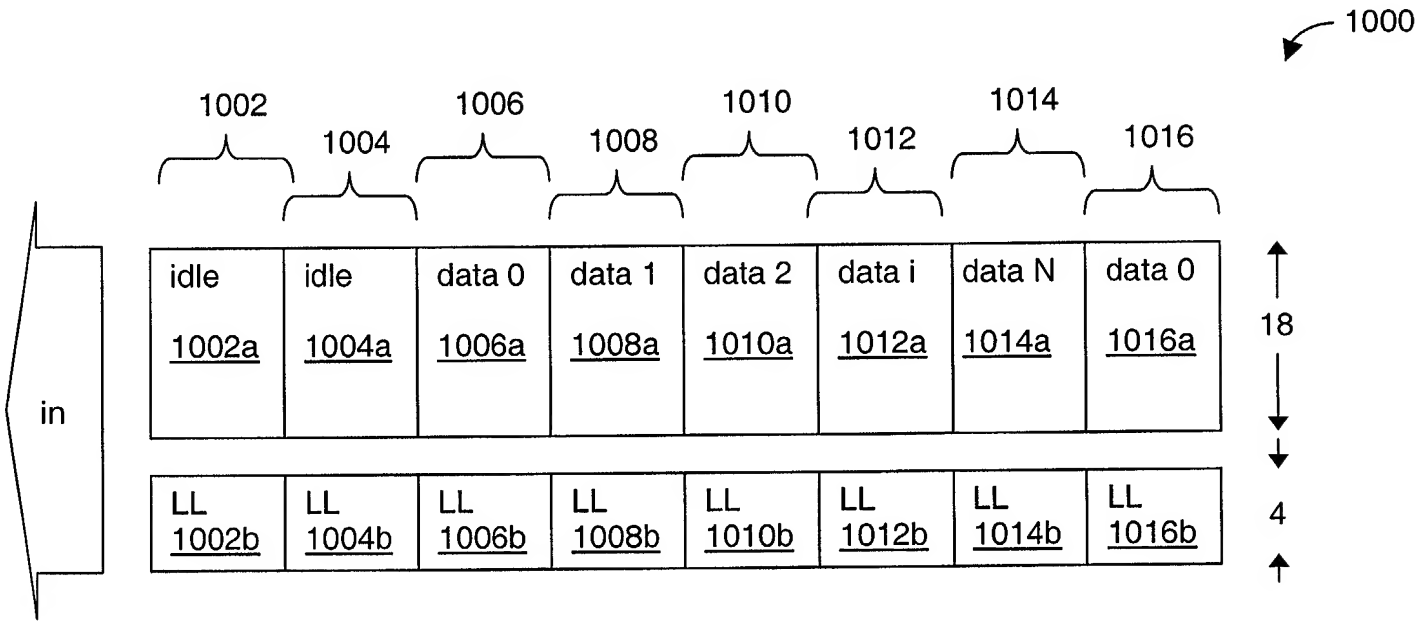
1000
1002
1004
1006
1008
1010
1012
1014
1016
idle
1002a
idle
1004a
data 0
1006a
data 1
1008a
data 2
1010a
data i
1012a
data N
1014a
data 0
1016a
18
in
LL
1002b
LL
1004b
LL
1006b
LL
1008b
LL
1010b
LL
1012b
LL
1014b
LL
1016b
4

FIG. 10

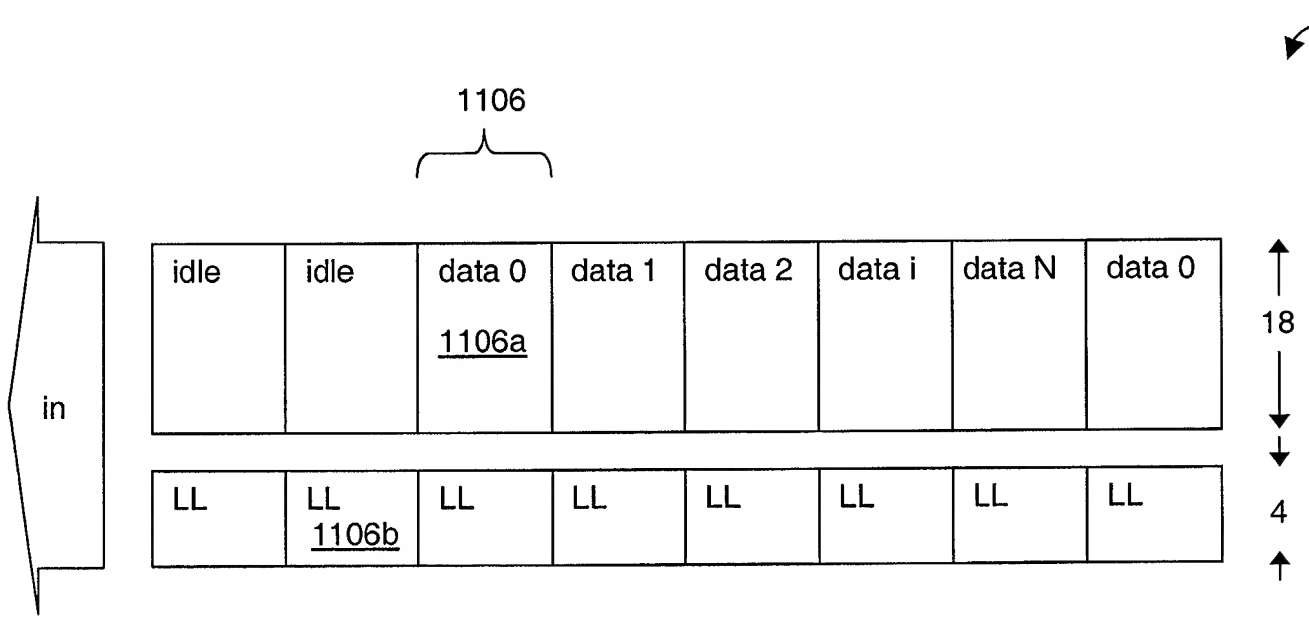
1100
1106
idle
idle
data 0
1106a
data 1
data 2
data i
data N
data 0
in
18
LL
LL
1106b
LL
LL
LL
LL
LL
LL
4

FIG. 11

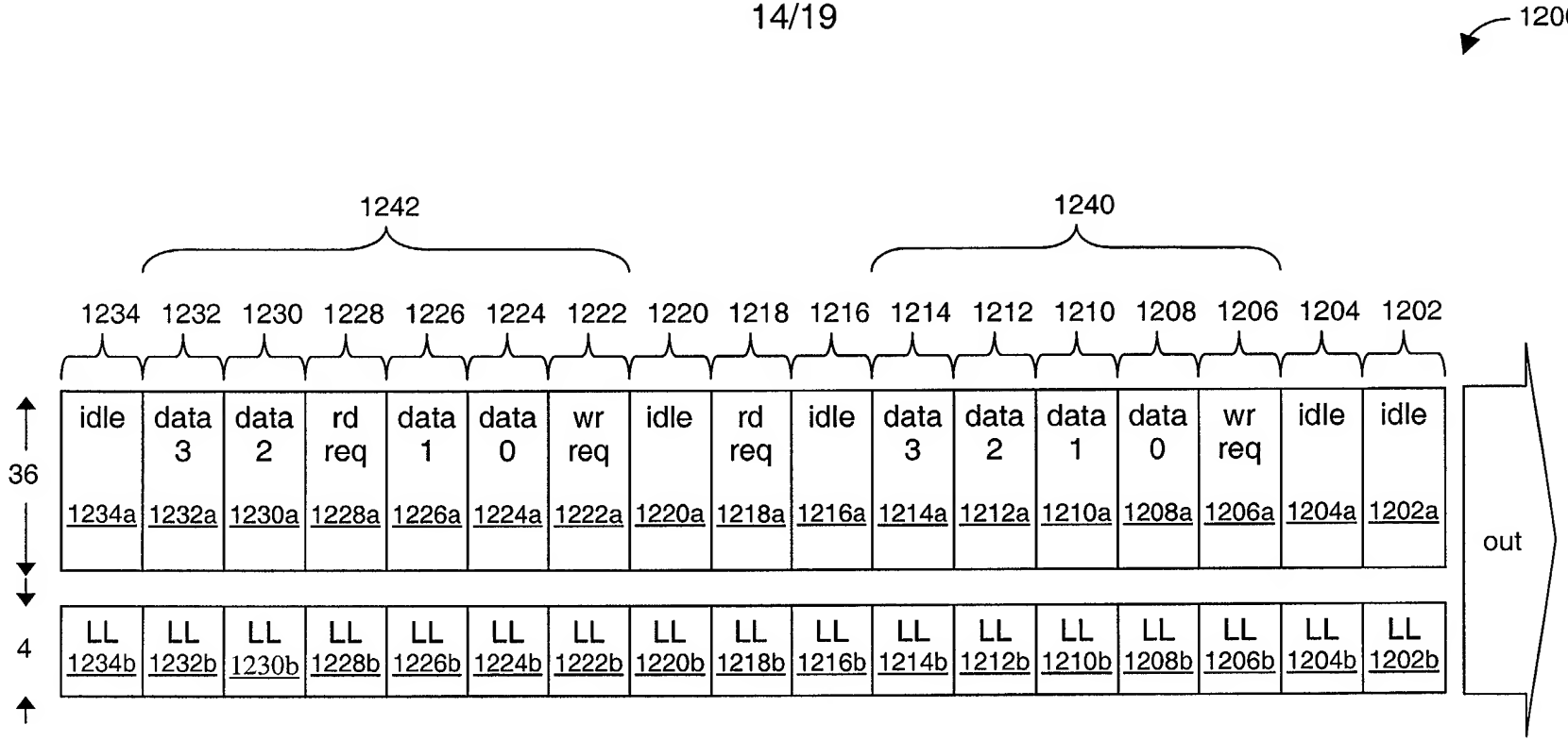
1200
1242
1240
1234 1232 1230 1228 1226 1224 1222 1220 1218 1216 1214 1212 1210 1208 1206 1204 1202
36
4
idle data 3 data 2 rd req data 1 data 0 wr req idle rd req idle data 3 data 2 data 1 data 0 wr req idle idle
1234a 1232a 1230a 1228a 1226a 1224a 1222a 1220a 1218a 1216a 1214a 1212a 1210a 1208a 1206a 1204a 1202a
LL 1234b LL 1232b LL 1230b LL 1228b LL 1226b LL 1224b LL 1222b LL 1220b LL 1218b LL 1216b LL 1214b LL 1212b LL 1210b LL 1208b LL 1206b LL 1204b LL 1202b
out

FIG. 12

1300

| ↓Transfer | BITS 17:0 |
|---|---|
| 0 | Lower Order Address Bits and Read/Write Command |
| 1 | Higher Order Address Bits and Early Read Indicator |
| 2 | Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, Stream ID, Size Bits, Cancel Command, Priority, etc. |
| 3 | |

FIG. 13

1400

| ↓Transfer | BITS 17:0 |
|---|---|
| 0 | Lower Order Address Bits and Read/Write Command |
| 1 | Higher Order Address Bits and Early Read Indicator |
| 2 | Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, Size Bits, etc. |
| 3 | |

FIG. 14

1500

| ↓Transfer | BITS 17:0 |
|---|---|
| 0 | Lower Order Configuration Address Bits and Read/Write Command |
| 1 | Higher Order Configuration Address Bits and Early Read Indicator |
| 2 | Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, etc. |
| 3 | |

FIG. 15

1600

| LL signals | Transfers 0:3 |
|---|---|
| 0 | Info and Check Bits |
| 1 | Header, Tail, and Check Bits |
| 2 | Extended Mode Bits |
| 3 | |

FIG. 16

1700

| LL signals | Transfers 0:3 |
|---|---|
| 0 | Type and Check Bits |
| 1 | |
| 2 | Info and Check Bits |
| 3 | |

FIG. 17

1800

| LL signals | Transfers 0:3 |
|---|---|
| 0 | Tag, Control, and Check Bits |
| 1 | |
| 2 | Tag, Info, and Check Bits |
| 3 | |

FIG. 18

1900

FIG. 19

2000

LL signal

FIG. 20